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Design and Implementation of 8421 Code to Unit Distance Code Using Reversible Logic Gates

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Abstract: *In recent technologies reversible logic is implemented in varies application fields. Programmable Logic Device (PLD) is a flexible architecture used for implementing digital circuits. For military applications code converters are mainly used to maintain high secrecy of data. In proposed work, the design of code converters are implemented in Programmable Logic Array (PLA) and Programmable Array Logic (PAL) techniques by using Fredkin and Feynman gate. By implementing this reversible gate quantum cost, garbage output, area, power, delay can be minimized. The code converters are designed and simulated using Xilinx software and implemented on FPGA SPARTAN 3.*

I. Introduction

In current VLSI Technology, Power Consumption is a very important factor for consideration. By using Reversible logic, power consumption and heat dissipation can be minimized. Power consumption is very less in reversible logic circuits is compared to irreversible logic circuits. Reversible Logic finds its own application in Quantum computing, Nano- technology, Optical computing, Computer graphics and Low Power VLSI. Ralf Launduer told that heat dissipation in irreversible circuits is not due to the process involved in the operation, but it is due to the bits that were erased during the logical computation process. He demonstrated Launder's principle which describes the lower theoretical limit of heat dissipation in logical computation. Launder's principle states that losing a single information bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant (approximately 1.38×10^{-23} J/K), T is Temperature and ln2 is natural algorithm of 2 (approximately 0.69315). The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits. It is necessary to notice that there is a direct relationship between the number of information bits erased to the amount of heat dissipated in the circuit. Later in 1973 C. H. Bennett described that the Power dissipation due to the bit loss can be overcome if each and every computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation, KTln2 Joules energy dissipation wouldn't occur if the Computation is carried out in reversible manner. He argued that for zero heat dissipation, the computation must be done in reversible manner. But if reversible logic is utilized to do logical computation, the heat dissipation will be less than KTln2 for one information bit in contrast to Launder. Thus computation done in reversible manner doesn't require erasing of bits [1].

II. Concept

The Reversible Logic involves the use of Reversible Gates consists of the same number of inputs and outputs i.e., there should be one to one mapping betweeninput vectors and output vectors. Thus the vector of input states can be always reconstructed from the vector of output state. Two constraints for reversible logic are,

1. Fan-out is not allowed (i.e., fan-out=1) and
2. Feed-back is not allowed.

In Reversible logic, the outputs are obtained with full knowledge of inputs. Reversible logic conserves information about Garbage outputs, Number of gates, Quantum cost, constant inputs are used to estimate the performance of reversible circuits. Garbage outputs are the extra outputs which helps to make inputs and outputs equal in order to maintain reversibility. The unused output are not considered into account since no operations are involved.Number of gates count is not a good metric since more number of gates can be taken together to form a new gate. Quantum Cost is the number of elementary or primitive gates needed to implement the gate, the number of reversible gates (1×1 or 2×2) required to construct the circuit. The main objective of reversible logic theory is the reversible function, which is defined as, reversible circuit has the same number of input and

output wires. Every output pattern has a unique pre-image. The reversible circuit with n inputs is called an n × n circuit.

Features of a reversible logic circuit are,

1. Minimum input constants.
2. Minimum number of garbage outputs.
3. Minimum number of reversible gate.

III. Reversible Logic Gate

The reversible logic gate consists of same number of inputs and outputs as shown in the figure1. The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

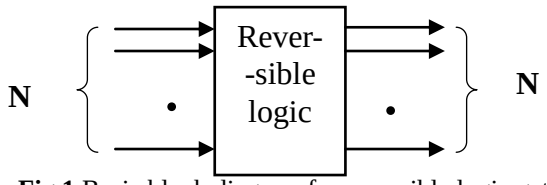
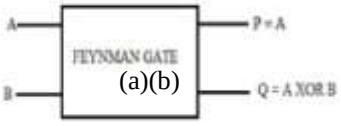


Fig.1 Basic block diagram for reversible logic gate

1.FEYNMAN GATE (CNOT): Feynman gate is a 2*2 one through reversible gate, it also called as controlled swap gate. The input vector is I (A, B) is mapping to the output vector is O (P, Q) outputs are defined as

- P=A,
- Q=A ⊕ B.

Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Fan-out is not allowed in reversible logic. This gate is useful for duplication of the required outputs.

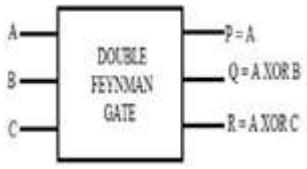


A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig.2 (a) Block diagram of Feynman Gate and (b) Truth Table of Feynman Gate

2.DOUBLE FEYNMAN GATE (DFG): Double Feynman gate is a 3*3 reversible gate. The input vector is I (A, B, C) is mapping to the output vector is O (P, Q, R). The quantum cost of this gate is 2 and its output is defined as,

- P=A,
- Q=A ⊕ B and
- R=A ⊕ C.



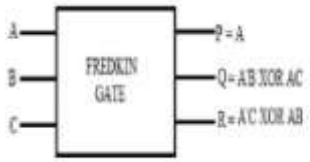
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

(a) (b)

Fig.3 (a) Block diagram of Double Feynman Gate and (b) Truth Table of Double Feynman Gate

3.FREDKIN GATE (FRG): Fredkin gate is a 3*3 reversible gate. The input vector is I (A, B, C) is mapping to the output vector is O (P, Q, R). Quantum cost of a Fredkin gate is 5.The output is defined as,

- P=A,
- Q=A′B ⊕ AC and
- R=A′C ⊕ AB.



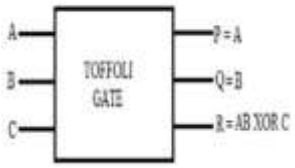
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

(a) (b)

Fig.4 (a) Block diagram of Fredkin Gate and (b) Truth Table of Fredkin Gate

4. TOFFOLI GATE (TG): Toffoli gate is a 3*3 reversible gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The quantum cost of this gate is 5 and the output is defined as,

- P=A,
- Q=B and
- R=AB ⊕ C.



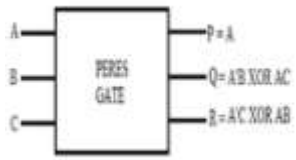
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

(a) (b)

Fig.5 (a) Block diagram of Toffoli Gate and (b) Truth Table of Toffoli Gate

5. PERES GATE (PG): Peres gate is a 3*3 reversible gate. The input vector is I (A, B, C) is mapping to the output vector is O (P, Q, R). The quantum cost for this gate is 4 and the output is defined as,

- P=A,
- Q=A ⊕ B
- R=AB ⊕ C.



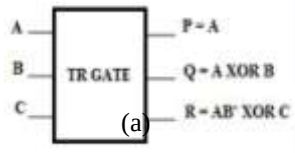
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

(a) (b)

Fig.6 (a) Block diagram of Feynman Gate and (b) Truth Table of Feynman Gate

6. TR GATE: TR gate is a 3*3 reversible gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The quantum cost of TRG gate is given by 4 and the output is defined as,

- P=A,
- Q=A ⊕ B and
- R=~A&B.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

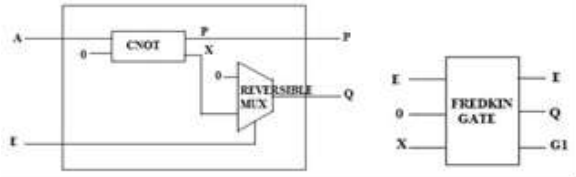
(a) (b)

Fig.7 (a) Block diagram of TR Gate and (b) Truth Table of TR Gate

IV. Proposed Method

The Programmable Logic Array (PLA) and Programmable Array Logic (PAL) was designed using Fredkin and Feynman gate based binary to gray code converter.The PLA consists of two levels of logic gates, an array of AND gates and an array of OR gates, both arrays are user programmable by using fuse. In PLA structure, fuse is replaced with reversible Fredkin gate and reversible Feynman gate is shown in figure. The Feynman reversible gate acts as a duplicating circuit. It duplicates the output line into two output lines out of

which one output line drives the next circuit and the other drives the second input of 2×1 reversible multiplexer. The first input of reversible multiplexer is grounded so that when the enable signal 'E' is low it acts as an 'off' switch. The reversible multiplexer is made of Fredkin gate as shown in the below figure.



(a) (b)

Fig.8 (a)Reversible Fuse and (b) Reversible MUX

The PAL consists of fixed OR gates array and programmable AND gate array. Contemporary to irreversible PAL, the fuses are replaced with programmable reversible fuses and the fixed connections are replaced with the CNOT gates as shown in the figure11. The 'P' output of fuse drives the subsequent fuse and the 'Q' output of fuse drives the input of AND gate as shown in figure13. The output of AND gate drives the fixed connections i.e., CNOT gate. The 'P' output of CNOT gate drives the next fixed connection and the 'Q' output of CNOT drives the input of OR gate.

In proposed work the reversible PLA and PAL has been designed based on the operation of Binary to Gray code converter using Reversible AND array and Reversible OR array. Binary to Gray code converter to convert binary values into gray code values it having four binary inputs (i.e B1,B2,B3,B4) and four gray code outputs (i.e G1,G2,G3,G4) and this equations are given below.

$$G1 = \overline{B2}\,B1 + B2\overline{B1} \quad \text{----------(Eqn 1)}$$

$$G2 = B3\overline{B2} + \overline{B3}B2 \quad \text{---------- (Eqn 2)}$$

$$G3 = \overline{B4}B3 + B4\,\overline{B3} \quad \text{---------- (Eqn 3)}$$

$$G4 = B4 \quad \text{---------- (Eqn 4)}$$

The circuit diagram of PAL is shown in Fig.9 it consists of 10 CNOT gate, 13 fuse, 6 Reversible AND gate and 4 Reversible OR gate. In that AND array is programmable and OR array is fixed. Therefore fuses are used to program the device. The G1 equation is got by performing the exclusive OR operation between the binary values B2 and B1 is given in Eqn 1.similary the G2 and G3 equations are got by performing the same operation is given in Eqn 2 and Eqn 3 respectively. Then the G4 is directly get from the binary value B4 is given in Eqn 4.

The binary input is given to CNOT gate, it consist of two input and two output. The CNOT gate performs the complement operation, so it complement the received binary input and give the complemented output to the fuse as input. The fuse perform its operation and its output is given to the reversible AND gate. The output of the reversible AND gate is given to the CNOT gate as input. And finally the output of the CNOT gate is applied to the reversible OR gate and the output is taken.

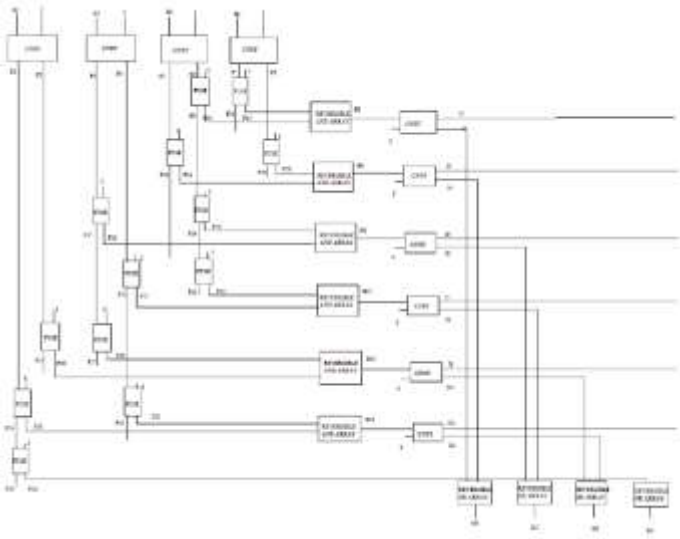


Fig.9 Block diagram of Reversible PAL to perform Binary to Gray code operations

The similar operation of PAL is performing in PLA. In PLA both AND array and OR array are programmable. Fig.10 shows the block diagram of Reversible PLA to perform Binary to Gray Code operations. The binary input is given to CNOT gate, it consist of two input and two output. The CNOT gate performs the complement operation, so it complement the received binary input and give the complemented output to the fuse as input. The fuse perform its operation and its output is given to the reversible AND gate. The output of the reversible AND gate is given to the fuse as input. And finally the output of the fuse is applied to the reversible OR gate and the output is taken.

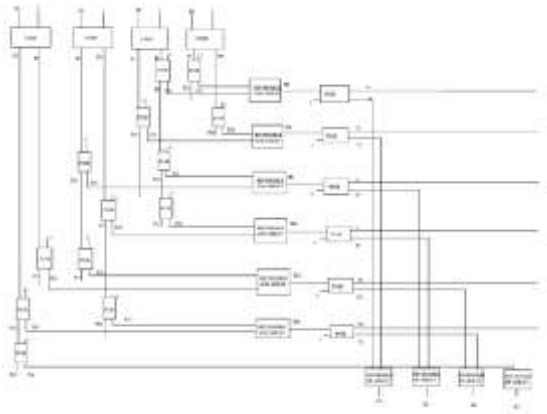


Fig.10 Block diagram of Reversible PLA to perform Binary to Gray code operations

V. Simulation Results Of Proposed Circuits

1. **REVERSIBLE PROGRAMMABLE ARRAY LOGIC**

The binary code converter equations are implemented using PAL. The RTL schematic and output waveform for PAL is shown in figure 11 and figure 12 respectively.

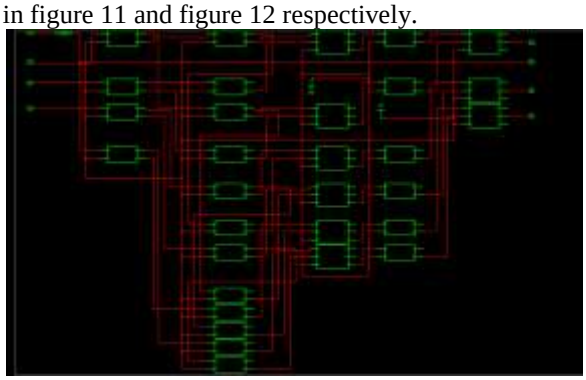


Fig.11 RTL Schematic of PAL in Binary to gray code

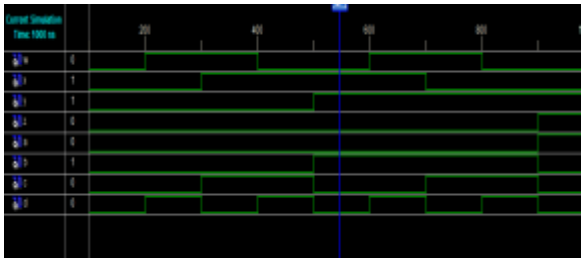


Fig.12 Output waveform of PAL in Binary to Gray code

2. Reversible programmable logic array

The binary code converter equations are implemented using PLA. The RTL schematic and output waveform for PLA is shown in figure 13 and figure 14 respectively.

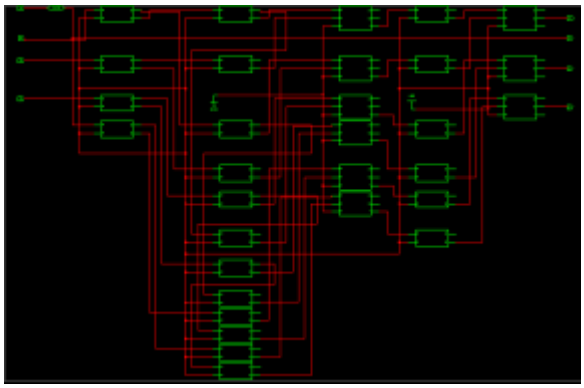


Fig.13 RTL Schematic of PLA in Binary to gray code

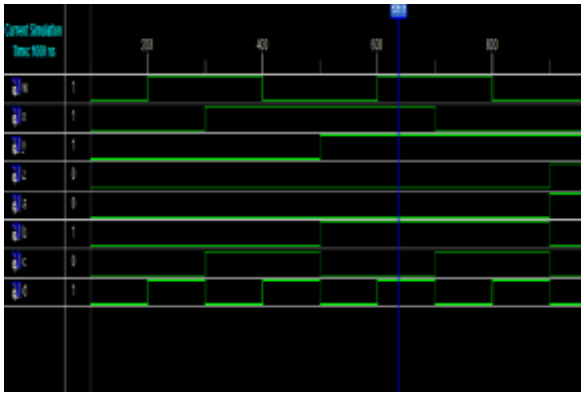


Fig.14 Output waveform of Binary to Gray code in PLA

Binary to gray code converter has been implemented with the help of FPGA SPARTAN 3 kit. It shows the output for the both PLA and PAL is shown in figure 15. If the quantum cost, garbage output, area and power can be calculated if it is shown in table 1.

Binary to gray	Quantum cost	Garbage output	Area	Power
PLA	157	34	47	834.233 nW
PAL	150	34	47	834.233 nW

Table.1 Parameter analysis

Fig.15 Implemetation of Binary to gray code converter in PLA using FPGA kit.

VI. Conclusion

The code converter are implemented with PLA and PAL technique using Fredkin and Feynman gate efficiently. The achieved quantum cost for PLA and PAL is 157 and 150 respectively and the garbage output for both PLA and PAL is 34. This code converter technique has been implemented on FPGA SPARTAN 3.

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